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ARM Accredited Engineer

ARM EN0-001

Version Demo

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QUESTION NO: 1

Which THREE of the following items should be preserved by software when entering dormant mode? (Choose three)

A. Current Program Status Register (CPSR)

B. Contents of the Level 2 data cache

C. The Floating Point Status and Control Register (FPSCR)

D. All User mode general-purpose registers

E. The CP15 Multiprocessor Affinity Register

F. Contents of the Level 1 data cache

ANSWER: A C D

QUESTION NO: 2

In an experiment, the time taken for an application to complete a given task is measured using a stopwatch. Which THREE of the following make up the total time? (Choose three)

A. The time spent waiting for I/O operations

B. The time taken to download the program via the debugger

C. The time taken for memory accesses

D. The time taken for the CPU to execute instructions

E. The time taken to compile the source code

F. The time taken to perform instruction tracing

ANSWER: A C D

QUESTION NO: 3

The following C function is compiled with hard floating point linkage.

float function(int a, float b, int c, float d);

Which register is used to pass argument c?

A. R0

B. R1

C. R2

D. R3

ANSWER: B

QUESTION NO: 4

Processors which implement the ARMv7-A architecture can be configured to allow unaligned memory access. Unaligned accesses have a number of advantages, disadvantages, and limitations.

Which TWO of the following statements are true? (Choose two)

A. Unaligned accesses may take more cycles to execute than aligned accesses

B. Unaligned loads and stores are necessary for accessing fields in packed structures

C. A program compiled using unaligned accesses can be safely executed on all ARMv7-A devices

D. If the relevant control register setting is enabled all loads and stores can function from unaligned addresses

E. Unaligned accesses can only be made to Normal memory

ANSWER: A E

QUESTION NO: 5

What is an "Entry point" in an application?

A. A place where execution can start

B. The location of the main () function

C. The lowest address contained in a program image

D. A location where the linker can store additional information

ANSWER: A

QUESTION NO: 6

In which of the following scenarios would cache maintenance operations be necessary in an ARMv7 system?

A. Before executing code that uses the NEON instruction set

B. Before handling an interrupt request raised by an external device

C. Before checking the status of a semaphore

D. Before reading cacheable memory that has been written to by an external bus master

ANSWER: D

QUESTION NO: 7

When an ARMv7-A MPCore system is in SMP mode, which of the following TWO operations can the processor handle automatically? (Choose two)

A. Coherency management between all L1 data caches

B. Broadcast of some inner-shared cache and TLB maintenance operations

C. Broadcast of some outer-shared cache and TLB maintenance operations

D. Coherency management between all L1 instruction caches

E. Coherency management between all external caches

ANSWER: A B

QUESTION NO: 8

Which of the following features was added in version 2 of the ARM Architecture Advanced SIMD extensions?

A. Additional quadword registers

B. Support for double precision floating-point arithmetic

C. Fused Multiply-Accumulate (Fused MAC) instructions

D. Support for polynomials

ANSWER: C

QUESTION NO: 9

Which TWO of the following interrupt types does a Generic Interrupt Controller (GIC) support? (Choose two)

A. Interrupt from a private peripheral to a processor

B. Interrupt from a processor to a private peripheral

C. Interrupt from a shared peripheral to a processor

D. Interrupt from a processor to a shared peripheral

E. Interrupt from a private peripheral to a shared peripheral

F. Interrupt from a shared peripheral to a private peripheral

ANSWER: A C

QUESTION NO: 10

The disassembly of a program written in C shows calls to the function__aeabi_fadd. Which one of these compiler floating point options could have been used?

A. Hard floating-point linkage

B. Soft floating-point linkage without floating-point hardware

C. Hard floating-point linkage with optimization for space

D. Soft floating-point linkage with floating-point hardware

ANSWER: B

QUESTION NO: 11

To return from a Data Abort handler and re-execute the aborting instruction, what value should be loaded to the PC?

A. PC=LR

B. PC=LR44

C. PC=LR-4

D. PC=LR-8

ANSWER: D

QUESTION NO: 12

Which TWO of the following options can the ARM Compiler (armcc) directive__packed be used for? (Choose two)

A. To tell the compiler to use only Thumb code

B. To tell the compiler to produce code of minimum size

C. To tell the compiler to use the v6 SIMD pack/unpack instructions

D. To tell the compiler that an object can be on an unaligned address

E. To tell the compiler not to perform padding inside structures

ANSWER: D E

QUESTION NO: 13

A development board is supplied with a Board Support Package (BSP) for a particular operating system. Which TWO of these items would you expect to find in the BSP? (Choose two)

A. Power supply and electrical cables

B. Debugging hardware and software solution

C. System on chip peripheral driver source code

D. Boundary scan protocol definition

E. Boot code for board-specific devices

ANSWER: C E

QUESTION NO: 14

The effect of clicking the Stop button in a debugger is to:

A. Put the processor(s) into debug state.

B. Force the processor to execute a BKPT instruction

C. Hold the processor in a Reset condition

D. Re-initialize the memory contents.

ANSWER: A

QUESTION NO: 15

The following pseudocode sequence shows a flag being set to indicate that new data is ready to be read by another thread:

data = 123;

ready = true;

Assuming that the reader threads may execute on any other core of a multicore system, which of the following is the most efficient memory barrier to place between the two writes to prevent them being observed in the opposite order?

A. DSBSY

B. DSBST

C. DMBSY

D. DMBST

ANSWER: D